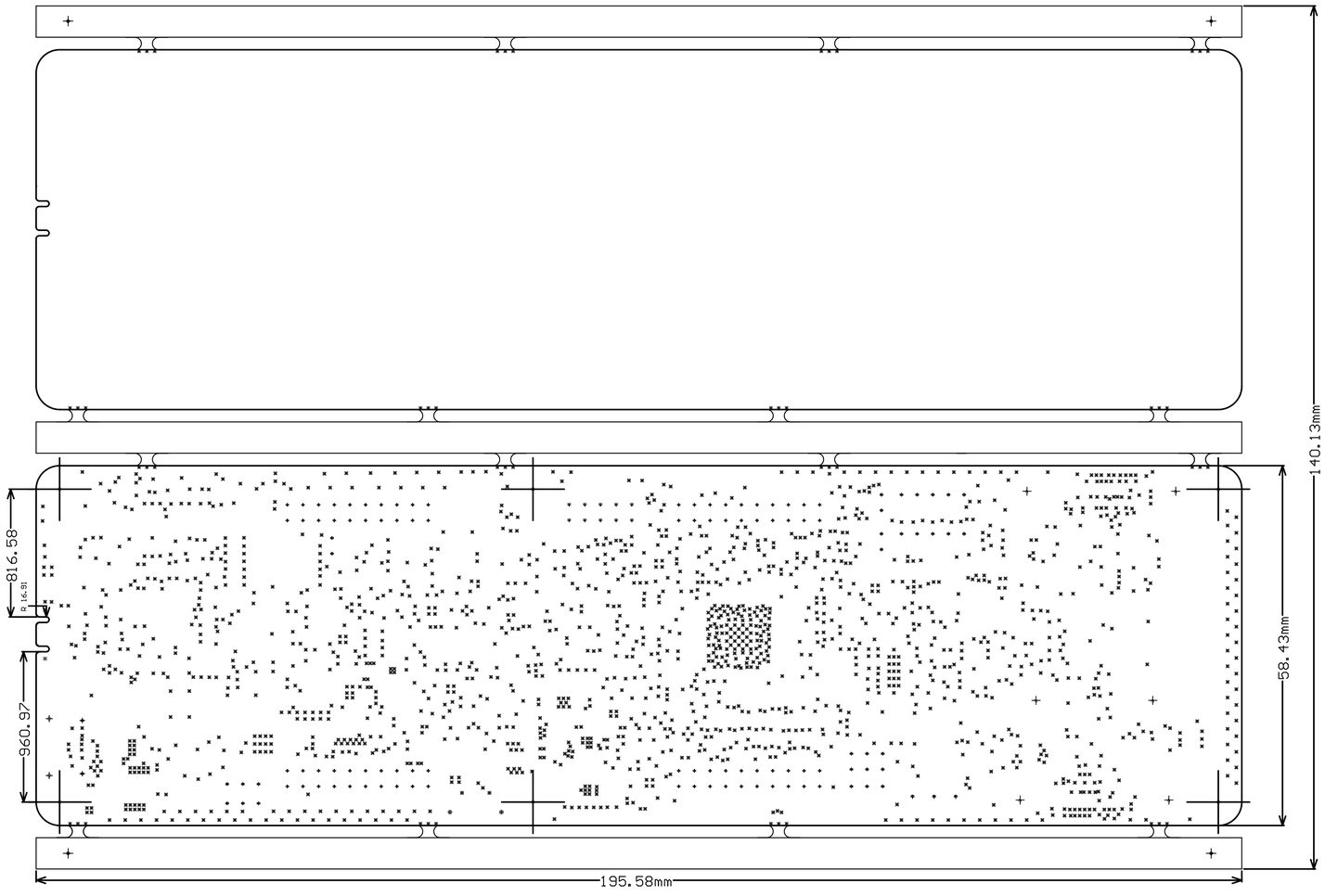
Symbol	Quantity	Finished Hole Size	Hole Length	Plated	Hole Tolerance (+)	Hole Tolerance (-)
⊠	1816	8.00mil (0.203mm)	-	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
□	2	23.62mil (0.600mm)	51.18mil (1.300mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
⧈	2	25.59mil (0.650mm)	29.53mil (0.750mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
⌑	48	32.00mil (0.813mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)
▽	10	39.37mil (1.000mm)	-	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
☼	31	40.00mil (1.016mm)	-	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
◇	80	40.16mil (1.020mm)	-	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
▼	3	47.24mil (1.200mm)	-	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
⊠	2	51.18mil (1.300mm)	29.53mil (0.750mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
✿	2	62.99mil (1.600mm)	23.62mil (0.600mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
○	2	82.68mil (2.100mm)	23.62mil (0.600mm)	PTH	3.00mil (0.076mm)	3.00mil (0.076mm)
⍝	6	108.00mil (2.743mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)
✪	10	126.00mil (3.200mm)	-	NPTH	3.00mil (0.076mm)	3.00mil (0.076mm)
	2014 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

SL#	TYPE	LAYER	WIDTH(Mils)	SPACE(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	MICROSTRIP	L1,L6	5.3	NA	50	L02,L05
02	EDGE COUPLED MICROSTRIP	L1,L6	4.2	5	90	L02,L05
03	EDGE COUPLED MICROSTRIP	L6	3.8	15	120	L05
04	STRIPLINE	L3	4.75	NA	50	L02/04
05	EDGE COUPLED STRIPLINE	L3	4	6	90	L02/04
06						

IMPEDANCE SPECIFICATIONS



LAYER STACK UP TABLE

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	ELECTRA EMP 110/5410-RED	1.00mil	4	
1	Top Layer	Copper Foil 18 microns	1.85mil		
	Dielectric 1	Iteq IT180A Prepreg 2113 RC58	3.55mil	4.13	
2	GND 1		1.26mil		
	Dielectric 3	Iteq IT180A 4 mil core 1/1	4.00mil	4.4	
3	SIG 1		1.26mil		
	Dielectric 5	Iteq IT180A Prepreg 106 RC71.5	1.86mil	3.79	
	Dielectric 7	Iteq IT180A Prepreg 1080 RC65	2.71mil	3.86	
	Dielectric1	Iteq IT180A 28 mil core H/H	28.00mil	4.53	
	Dielectric 8	Iteq IT180A Prepreg 1080 RC65	2.71mil	3.86	
	Dielectric 6	Iteq IT180A Prepreg 106 RC71.5	1.86mil	3.79	
4	PWR		1.26mil		
	Dielectric 4	Iteq IT180A 4 mil core 1/1	4.00mil	4.4	
5	GND 2		1.26mil		
	Dielectric 2	Iteq IT180A Prepreg 2113 RC58	3.55mil	4.13	
6	Bottom Layer	Copper Foil 18 microns	1.85mil		
	Bottom Solder	ELECTRA EMP 110/5410-RED	1.00mil	4	
	Bottom Overlay				

1000.00mil

DESIGN INFORMATION

MIN. TRACK WIDTH: 3.8 MIL
MIN. CLEARANCE: 4 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER
BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER
ARRAY/PANEL: ☒ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☐ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: AM261 Launchpad
DESIGNED FOR: .PRJ_Customer
FILE NAME: PROC193E2.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC193	REV: E2	SVN REV: 427 [Locally Modified]
LAYER NAME = M1 Board Outline M2 Board Dimensions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 24-01-2025 11:58:10	TEXAS INSTRUMENTS	

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:	LAYOUT BY:
Vijetha J, Kiran	.PCB_Layout
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.9.2.47